# Junha Ryu

**Office:** #1233, E3-2, KAIST

**E-mail:** junha.ryu@kaist.ac.kr / jnharyu@gmail.com

**LinkedIn:** www.linkedin.com/in/junharyu

**Homepage:** junharyu.github.io

## Research Interests

- My current research interests include **energy-efficient System-on-Chip design**, especially focused on **AI-powered AR/VR and 3D vision systems**. Over the past 4 years, I have participated in the design of 3 silicon chips related to artificial intelligence.
- **Research Topics (w/ Related Publication)**
  - ✓ **Neural Graphics Acceleration:** ISSCC'23, ASSCC'23, ISSCC'24
  - ✓ **3D Vision System:** ISSCC'22
  - ✓ **AR/VR System-on-Chip:** IEDM'21
  - ✓ **DNN Accelerator:** JSSC'21, HPCA'23

## Education

**KAIST**, Daejeon, Republic of Korea **Mar. 2022 - Present**

**Ph.D**. Candidate in School of Electrical Engineering

**Advisor:** Professor Hoi-Jun Yoo (IEEE Fellow)

**KAIST**, Daejeon, Republic of Korea **Mar. 2020 – Feb. 2022**

**M.S.** in School of Electrical Engineering

**Thesis:** *A CIS-based Action Recognition SoC with Self-Adjustable Frame Resolution for Always-on IoT Devices*

**Advisor:** Professor Hoi-Jun Yoo (IEEE Fellow)

**KAIST**, Daejeon, Republic of Korea **Mar. 2015 – Feb. 2020**

**B.S.** in School of Electrical Engineering

## Honors and Awards

- **Bronze Award,** 29th Samsung Humantech Paper Award **(2023.02) –** 2nd Author
- **Bronze Award,** 28th Samsung Humantech Paper Award **(2022.02) –** 4th Author
- National Science and Engineering Undergraduate Scholarship **(2017-2018)**

## Publications

**(C: Conference, J: Journal, P: Preprint)**

**[C-17]**

**NeuGPU: A Neural Graphics Processing Unit for Instant Modeling and Real-Time Rendering for Mobile AR/VR Devices**

**Junha Ryu**, Hankyul Kwon, Wonhoon Park, Zhiyong Li, Beomseok Kwon, Donghyeon Han, Dongseok Im, Sangyeob Kim, Hyungnam Joo, Minsung Kim, and Hoi-Jun Yoo

*IEEE Hot Chips Symposium* (**HCS**), 2024

**[C-16]**

**NeRF-Navi: A 93.6-202.9μJ/task Switchable Approximate-Accurate NeRF Path Planning Processor with Dual Attention Engine and Outlier Bit-Offloading Core**

Seryeong Kim, Seokchan Song, Wonhoon Park, **Junha Ryu**, Sangyeob Kim, Gwangtae Park, Soyeon Kim, and Hoi-Jun Yoo

*IEEE International Symposium on VLSI Technology and Circuits* (**S. VLSI**), 2024

**[C-15]**

**A Low-Power Neural Graphics System for Instant 3D Modeling and Real-Time Rendering on Mobile AR/VR Devices**

**Junha Ryu**, Hankyul Kwon, Wonhoon Park, Zhiyong Li, Beomseok Kwon, Donghyeon Han, Dongseok Im, Sangyeob Kim, Hyungnam Joo, Minsung Kim, and Hoi-Jun Yoo

*IEEE Symposium in Low-Power and High-Speed Chips* (**COOL CHIPS**), 2024

**[C-14]**

**A 8.81 TFLOPS/W Deep-Reinforcement-Learning Accelerator with Delta-Based Weight Sharing and Block-Mantissa Reconfigurable Pe Array**

Sanghyuk An, **Junha Ryu**, Gwangtae Park, and Hoi-Jun Yoo

*IEEE International Symposium on Circuits and Systems* (**ISCAS**), 2024

**[C-13]**

**NeuGPU: A 18.5 mJ/Iter Neural-Graphics Processing Unit for Instant-Modeling and Real-Time Rendering with Segmented-Hashing Architecture**

**Junha Ryu**, Hankyul Kwon, Wonhoon Park, Zhiyong Li, Beomseok Kwon, Donghyeon Han, Dongseok Im, Sangyeob Kim, Hyungnam Joo, and Hoi-Jun Yoo

*IEEE International Solid-State Circuits Conference* (**ISSCC**), 2024

**[C-12]**

**A 33.58 FPS Embedding based Real-time Neural Rendering Accelerator with Switchable Computation Skipping Architecture on Edge Device**

Jongjun Park, Donghyeon Han, **Junha Ryu**, Dongseok Im, Gwangtae Park, and Hoi-jun Yoo

*IEEE Asian Solid-State Circuits Conference* (**ASSCC**), 2023

**[C-11]**

**A 5.99 TFLOPS/W Heterogeneous CIM-NPU Architecture for an Energy Efficient Floating-Point DNN Acceleration**

Wonhoon Park, **Junha Ryu**, Sangjin Kim, Soyeon Um, Wooyoung Jo, Sangyoeb Kim, and Hoi-Jun Yoo

*IEEE International Symposium on Circuits and Systems* (**ISCAS**), 2023

**[C-10]**

**A 15.9 mW 96.5 fps Memory-Efficient 3D Reconstruction Processor with Dilation-based TSDF Fusion and Block-Projection Cache System**

Hankyul Kwon, Gwangtae Park, **Junha Ryu**, Wooyoung Jo, and Hoi-Jun Yoo

*IEEE International Symposium on Circuits and Systems* (**ISCAS**), 2023

**[C-9]**

**A Low-power Neural 3D Rendering Processor with Bio-inspired Visual Perception Core and Hybrid DNN Acceleration**

Donghyeon Han, **Junha Ryu**, Sangyeob Kim, Sangjin Kim, Jongjun Park, and Hoi-Jun Yoo

*IEEE Symposium in Low-Power and High-Speed Chips* (**COOL CHIPS**), 2023

**[C-8]**

**Sibia: Signed Bit-slice Architecture for Dense DNN Acceleration with Slice-level Sparsity Exploitation**

Dongseok Im, Gwangtae Park, Zhiyong Li, **Junha Ryu**, and Hoi-Jun Yoo

*IEEE International Symposium on High-Performance Computer Architecture* (**HPCA**), 2023

**[C-7]**

**MetaVRain: A 133mW Real-Time Hyper-Realistic 3D-NeRF Processor with 1D-2D Hybrid-Neural Engines for Metaverse on Mobile Devices**

Donghyeon Han, **Junha Ryu**, Sangyeob Kim, Sangjin Kim, and Hoi-Jun Yoo

*IEEE International Solid-State Circuits Conference* (**ISSCC**), 2023

**[C-6]**

**DSPU: A 281.6 mW Real-Time Deep Learning-Based Dense RGB-D Data Acquisition with Sensor Fusion and 3D Perception System-on-Chip**

Dongseok Im, Gwangtae Park, Zhiyong Li, **Junha Ryu**, Sanghoon Kang, Donghyeon Han, Jinsu Lee, Wonhoon Park, Hankyul Kwon, and Hoi-Jun Yoo

*IEEE Hot Chips Symposium* (**HCS**), 2022

**[C-5]**

**A Low-power and Real-time 3D Object Recognition Processor with Dense RGB-D Data Acquisition in Mobile Platforms**

Dongseok Im, Gwangtae Park, **Junha Ryu**, Zhiyong Li, Sanghoon Kang, Donghyeon Han, Jinsu Lee, and Hoi-Jun Yoo

*IEEE Symposium in Low-Power and High-Speed Chips* (**COOL CHIPS**), 2022

**[C-4]**

**DSPU: A 281.6 mW real-time depth signal processing unit for deep learning-based dense RGB-D data acquisition with depth fusion and 3D bounding box extraction in mobile platforms**

Dongseok Im, Gwangtae Park, Zhiyong Li, **Junha Ryu**, Sanghoon Kang, Donghyeon Han, Jinsu Lee, and Hoi-Jun Yoo

*IEEE International Solid-State Circuits Conference* (**ISSCC**), 2022

**[C-3]**

**AI SoCs for AR/VR user-interaction (Invited)**

**Junha Ryu**, Dongseok Im, and Hoi-Jun Yoo

*IEEE International Electron Devices Meeting* (**IEDM**), 2021

**[C-2]**

**A 0.82 μW CIS-Based Action Recognition SoC With Self-Adjustable Frame Resolution for Always-on IoT Devices**

**Junha Ryu**, Gwangtae Park, Dongseok Im, Ji-Hoon Kim, and Hoi-Jun Yoo

*IEEE International Symposium on Circuits and Systems* (**ISCAS**), 2021

**[C-1]**

**GANPU: A Versatile Many-Core Processor for Training GAN on Mobile Devices with Speculative Dual-Sparsity Exploitation**

Sanghoon Kang, Donghyeon Han, Juhyoung Lee, Dongseok Im, Sangyeob Kim, Soyeon Kim, **Junha Ryu**, and Hoi-Jun Yoo

*IEEE Hot Chips Symposium* (**HCS**), 2020

**[J-7]**

**A 8.81 TFLOPS/W Deep-Reinforcement-Learning Accelerator with Delta-based Weight Sharing and Block-Mantissa Reconfigurable PE Array**

Sanghyuk An, **Junha Ryu**, Gwangtae Park, and Hoi-Jun Yoo

*IEEE Transactions on Circuits and Systems II: Express Briefs* (**TCAS-II**), 2024

**[J-6]**

**A Low-power AI-based 3D Rendering Processor with Hybrid DNN Computing**

Donghyeon Han, **Junha Ryu**, Sangyeob Kim, Sangjin Kim, Jongjun Park, and Hoi-Jun Yoo

*IEEE Micro*, 2023

**[J-5]**

**MetaVRain: A Mobile Neural 3-D Rendering Processor With Bundle-Frame-Familiarity-Based NeRF Acceleration and Hybrid DNN Computing**

Donghyeon Han, **Junha Ryu**, Sangyeob Kim, Sangjin Kim, Jongjun Park, and Hoi-Jun Yoo

*IEEE Journal of Solid-State Circuits* (**JSSC**), 2023

**[J-4]**

**A Mobile 3D Object Recognition Processor with Deep Learning-based Monocular Depth Estimation**

Dongseok Im, Gwangtae Park, Zhiyong Li, **Junha Ryu**, Sanghoon Kang, Donghyeon Han, Jinsu Lee, Wonhoon Park, Hankyul Kwon, and Hoi-Jun Yoo

*IEEE Micro*, 2023

**[J-3]**

**DSPU: An Efficient Deep Learning-Based Dense RGB-D Data Acquisition With Sensor Fusion and 3-D Perception SoC**

Dongseok Im, Gwangtae Park, **Junha Ryu**, Zhiyong Li, Sanghoon Kang, Donghyeon Han, Jinsu Lee, Wonhoon Park, Hankyul Kwon, and Hoi-Jun Yoo

*IEEE Journal of Solid-State Circuits* (**JSSC**), 2022

**[J-2]**

**GANPU: An energy-efficient multi-DNN training processor for GANs with speculative dual-sparsity exploitation**

Sanghoon Kang, Donghyeon Han, Juhyoung Lee, Dongseok Im, Sangyeob Kim, Soyeon Kim, **Junha Ryu**, and Hoi-Jun Yoo

*IEEE Journal of Solid-State Circuits* (**JSSC**), 2021

**[J-1]**

**A 0.82 μW CIS-Based Action Recognition SoC With Self-Adjustable Frame Resolution for Always-on IoT Devices**

**Junha Ryu**, Gwangtae Park, Dongseok Im, Ji-Hoon Kim, and Hoi-Jun Yoo

*IEEE Transactions on Circuits and Systems II: Express Briefs* (**TCAS-II**), 2021

**[P-1]**

**Extension of direct feedback alignment to convolutional and recurrent neural network for bio-plausible deep learning**

Donghyeon Han, Gwangtae Park, **Junha Ryu**, and Hoi-Jun Yoo

*arXiv preprint*, 2020

## Invited Talks

**Google, San Diego, CA (Host: Kangmin Lee)** **Feb. 2024**

"NeuGPU: A 18.5 mJ/Iter Neural-Graphics Processing Unit for Instant-Modeling and Real-Time Rendering with Segmented-Hashing Architecture"

**Apple Inc., Cupertino, CA (Host: Youchang Kim)** **Feb. 2024**

"NeuGPU: A 18.5 mJ/Iter Neural-Graphics Processing Unit for Instant-Modeling and Real-Time Rendering with Segmented-Hashing Architecture"

## Activities

**Student Representative, Semiconductor System Lab**, KAIST **Jul. 2023 – Jun. 2024**

**Research Intern, Semiconductor System Lab,** KAIST **Dec. 2018 – Feb. 2020**

**Visiting Student, Technical University of Denmark (DTU),** Lyngby, Denmark **Feb. 2018 – Aug. 2018**

## Teaching Experience

**Teaching Assistant,** Introduction to Electronics Design Lab (EE305), KAIST, Fall 2021

**Teaching Assistant**, EE Co-op Program (Samsung DRAM Design Team), KAIST, Summer 2021

**Teaching Assistant,** Electronics Design Lab <Circuit and System> (EE405), KAIST, Spring 2021

**Teaching Assistant,** Introduction to Electronics Design Lab (EE305), KAIST, Fall 2020